UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,298	12/09/2003	Wagdi W. Abadeer	END920030103US1	3646

30449 7590 04/22/2005

SCHMEISER, OLSEN + WATTS
3 LEAR JET LANE
SUITE 201
LATHAM, NY 12110

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,298	ABADEER ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-16 and 18-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-16 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 03/21/05. A new ground of rejection is introduced as necessitated by amendment.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 6, 8, 11, 12, 14, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6844750) in view of Stubbs et al. (USP 6597619) (previously cited).

As to claims 1 and 15, Hsu et al.'s figure 12 shows a circuit comprising a current mirror (1206, 1208) coupled to a tunneling leakage monitor (1210), the tunneling leakage monitor including a tunneling leakage monitoring device (1210), the current mirror adapted to force a current through the tunneling leakage device to a predetermined current value, the current comprising only tunneling leakage current. Thus, figure 12 shows all limitations of the claim except for a voltage buffer coupled to the leakage monitor. However, Stubbs et al.'s figure 3 shows a buffer circuit for reducing output noise. Therefore, it would have been obvious to one having ordinary skill in the art to couple Stubbs et al.'s cirucit figure 3 to the output of Hsu et al.'s figure 12 for the purpose of reducing output noise. Thus, the modified Hsu et al.'s further shows a voltage buffer (Stubbs et al.'s 200) coupled to the leakage monitor, the voltage buffer

adapted to generate an output voltage based on a voltage level developed across the leakage monitoring device when the current is at the predetermined current value.

As to claims 6 and 19, the modified Hsu et al.'s figure 12 further shows a voltage regulator (Stubbs et al.'s 250) coupled to the voltage buffer, the voltage regulator adapted to supply a fixed voltage to a power distribution network of an integrated circuit chip based on the output voltage of the voltage buffer.

As to claim 8, the modified Hsu et al.'s figure 12 shows a method comprising: forcing a current (output of Hsu et al.'s 1208) of known value only through a dielectric layer of a tunneling current leakage monitor device (1210) to provide a voltage signal (Vsense); and regulating (bu using Stubbs et al.'s figure 3) on-chip power supply of the integrated circuit chip based on the voltage signal.

As to claim 11, the modified Hsu et al.'s figure 12 shows all limitations of the claim except for the step of performing a burn-in test of the integrated circuit chip while forcing the current of known value through a tunneling current leakage monitor device. However, it is notoriously well known in the art that bum-in test is for ensuring the circuit operates properly in a high voltage condition. Therefore, it would have been obvious to one having ordinary skill in the art to performing a burn-in test of the integrated circuit chip while forcing the current of known value through a tunneling current leakage monitor device for the purpose of ensuring the circuit operates properly in a high voltage condition.

As to claim 12, it is seen as an obvious design preference to select the current of known value is to be about equal to the tunneling leakage current of a worst-case process integrated circuit chip dependent upon particular environment of use to ensure optimum performance.

As to claim 14, it is inherent that the first value current in a burn-in operation of the integrated circuit is higher than a second current value in a normal operation because the supply voltage in a burn-in operation is higher than the supply voltage in a normal operation.

3. Claims 2, 3, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6844750) in view of Stubbs et al. (USP 6597619) and Maneatis (USP 6462527).

As to claims 2 and 16, the modified Hsu et al.'s figure 12 shows all limitations of the claim except for the current mirror includes an adjustable current source and means to adjust a current generated by the current source. However, it is notoriously well known in the art that adjustable current source is more flexible to generate desired current that a fix current source. Maneatis's figure 3 shows an adjustable current source with a large operation range. Therefore, it would have been obvious to one having ordinary skill in the art to use Maneatis' adjustable current source figure 3 for Hsu et al. et al.'s current source (1204) for the purpose of having more flexibility to select and generate desired current.

As to claim 3, the modified Hsu et al.'s reference further fail to show that the current source is a band gap current source. However, it is notoriously well known in the art that bandgap current source generates current independent of temperature. It would have been obvious to one having ordinary skill in the art to use bandgap current source to provide current to the Maneatis' current mirror circuit for the purpose of improving the performance of the circuit. Maneatis' figure 3 further shows that the means (the switches and the switch selection circuit, not shown, in Maniatis's figure 3) to adjust a current generated by the current source is a digital to analog converter.

As to claim 13, the output voltage of the buffer is varies depending on the number of switches that are closed. The value of the output voltage with only one closed switch is a nominal value. Thus, the voltage level of the on-chip power supply for the best case process integrated circuit is lowered when no switch is closed; and the voltage level of the on-chip power supply for the worst case process integrated circuit is raised when more than one switches are closed.

4. Claims 5, 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6844750) in view of Stubbs et al. (USP 6597619) and Maneatis (USP 6462527) and Shyr et al. (USP 6472897).

As to claims 5, 10 and 18, the modified Hsu et al.'s figure 12 shows all limitations of the claim except for fuse circuit controls the DAC. However, Shyr et al.'s figure 1 shows fuse circuit 14 controls the DAC. The benefit of using the fuse circuit is the output control signal irreversible when fuse is blown. Therefore, it would have been obvious to one having ordinary skill in the art to use fuse circuit to control the DAC in the modified Hsu et al.'s reference for the purpose of permanently closing or opening the switches in the DAC.

5. Claims 7, 9 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6844750) in view of Stubbs et al. (USP 6597619) and Persun et al. (US 2004/0236200).

As to claim 7, 9 and 20The modified Hsu et al.'s figure 12 fails to shows that leakage monitor device is a gate capacitor. However, Persun et al.'s figure 2A shows leakage monitor circuit using gate capacitor (215), instead of using transistor 115 in figure 1A, as a leakage

monitor device. Therefore, it would have been obvious to one having ordinary skill in the art to use gate capacitor for Hsu transistor 1210 for the purpose of saving space and cost.

As to claims 21 and 22, the modified Hsu et al.'s figure 12 shows that the source and drain of the gate capacitor are electrically tied together.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

April 20, 2005